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Box: PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

Attorney Reference: OKI 226

Re: New Patent Application of: Seiji ANDOH
Title: PACKAGE STRUCTURE FOR A SEMICONDUCTOR DEVICE

Sir:

Please find attached hereto an application for patent which includes:

[x] Specification, Claims and Abstract (15 pages)
[x] 5 Sheets of Drawings (Fig. 1 through Fig. 14)
[x] Inventor Declaration and Power of Attorney (1 Page)
[x] Assignment document with cover page (2 Pages)
[x] Fee (see formula below) Check Enclosed

Basic Fee $380/760	$ 760.00
Additional Fees:	
Total number of claims: 19 in excess of 20: 0 times $09/18	$ 00.00
Number of independent claims: 3 in excess of 3: 0 times $39/78	$ 00.00
Multiple Dependent Claims $130/260	$ 00.00
Recording Fee $40.	$ 40.00
TOTAL FEES FOR THE ABOVE APPLICATION	**$ 800.00**

In the event there is attached hereto no check, or a check for an insufficient amount, please charge the fee to our Account No. 18-0002 and notify us accordingly.

The rights of priority are claimed under 35 USC §119 of Japanese Application No. 10-232126, filed August 18, 1998.

FEE ENCLOSED: $ 760.00
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Respectfully submitted,

August 17, 1999
Date

Steven M. Rabin
Reg. No. 29,102

SMR:vap

PACKAGE STRUCTURE FOR A SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

The present invention relates to a package structure for a semiconductor device, and more particularly, it relates to a package structure having radiation solder bumps and connection solder bumps on a back surface of the package structure.

A conventional semiconductor device includes a package for covering a semiconductor chip, a substrate having a main surface on which the semiconductor chip is formed and radiation solder bumps and connection solder bumps formed on the back surface of the substrate.

The radiation solder bumps are formed in the center area of the back surface of the substrate. The connection solder bumps are formed in the peripheral area which surrounds the center area of the substrate. The connection solder bumps are electrically connected to electrodes of the semiconductor chip through conductive lines formed in the substrate. Therefore, the connection solder bumps have a function of terminals for connecting the semiconductor device to an outside circuit.

When the semiconductor device is mounted on a circuit board, the semiconductor device is subjected to a heat treatment (it is called as a reflow step). The circuit board has radiation pads located in corresponding position to the radiation solder bumps and connection pads located in corresponding position to the connection solder bumps. The radiation solder bumps and connection solder bumps are melted by the heat treatment so that both of the solder bumps are connected and joined to the pads, respectively. Therefore, the semiconductor device is fixed on the circuit board.

Each of the connection solder bumps should be connected to one of the connection pads independently. Therefore, the connection solder bumps are

formed with a predetermined pitch so that the adjacent connection solder bumps should not joined each other by the heat treatment (it is called as a solder bridge).

The radiation bumps which are not connected to the electrodes of the semiconductor chip are formed with the same pitch of the connection solder bumps. The heat energy generated by the semiconductor chip in the package is transferred to the circuit board through a thermal conduction part including the radiation bumps and radiation pads. The transferred heat energy is diffused in the circuit board and outgoing from the circuit board.

Since the radiation solder bumps are formed with the same pitch of the connection solder bumps, a cross sectional area of the thermal conduction part is relatively small and a coefficient of thermal conductivity thereof is low.

SUMMARY OF THE INVENTION

The present invention is done in consideration of the problems of the conventional semiconductor device. The object of the present invention is to provide a new and improved semiconductor device including radiation protrude electrodes which improve coefficient of thermal conductivity of the semiconductor device.

To solve the issues of the conventional semiconductor device, a package structure for a semiconductor device comprises a substrate having a main surface and a back surface, a semiconductor chip formed on the main surface of the substrate, a package covering the semiconductor chip, radiation protrude electrodes and connection protrude electrodes. The radiation protrude electrodes are formed on the back surface of the substrate in a chip area where said semiconductor chip is located. Each of the radiation protrude electrodes are formed with a first pitch so that the radiation protrude electrodes make one body joining layer when the package structure is subjected to a heat treatment. The connection protrude electrodes are formed on the back surface of the substrate in

a peripheral area of the chip area. Each of the connection protrude electrodes formed with a second pitch which is larger than the first pitch so that the connection protrude electrodes stay individual when the package structure is subjected to a heat treatment.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a side elevation view of a semiconductor device according to the first embodiment of the present invention;

Figure 2 is a bottom plan view of the semiconductor device according to the first embodiment of the present invention;

Figure 3 is a side elevation view of the semiconductor device and a circuit board according to the first embodiment of the present invention;

Figure 4 is an enlarged elevation view of the semiconductor device and the circuit board shown in Fig. 3;

Figure 5 is a fragmentary sectional view of the circuit board used in the first embodiment of the present invention;

Figure 6 is another fragmentary sectional view of the circuit board used in the first embodiment of the present invention;

Figure 7 is a side elevation view of a semiconductor device and a circuit board according to the second embodiment of the present invention;

Figure 8 is a bottom plan view of the semiconductor device according to the second embodiment of the present invention;

Figure 9 is an enlarged elevation view of the semiconductor device and the circuit board shown in Fig. 7;

Figure 10 is a sectional view of a semiconductor device according to the third embodiment of the present invention;

Figure 11 is a sectional view of a semiconductor device according to the fourth embodiment of the present invention;

Figure 12 is a sectional view of a semiconductor device according to the fifth embodiment of the present invention;

Figure 13 is a sectional view of a semiconductor device according to the sixth embodiment of the present invention; and

Figure.14 is a sectional view of the semiconductor device according to the seventh embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The preferred embodiment of the present invention will be explained in detail with reference to the accompanying drawings.

The first embodiment is described referring to Figs. 1 through 6. Figure 1 is a side elevation view of a semiconductor device according to the first embodiment of the present invention. A semiconductor device 10 according to the first embodiment of the present invention includes a package 11 in which a semiconductor chip (not shown in Fig. 1) is molded. The semiconductor device 10 includes a substrate 11a having a main surface on which the package 11 and the semiconductor chip is formed. The semiconductor device 10 further includes radiation solder bumps 13 and connection solder bumps 14 formed on a back surface of the substrate 11a.

As shown in Fig. 2, the radiation solder bumps 13 are located in the central region of the back surface of the substrate 11a. The connection solder bumps 14 are located in a peripheral region which surrounds the central region of the back surface of the substrate 11a. The connection solder bumps 14 are electrically connected to electrodes of the semiconductor chip through conductive lines formed in the substrate, respectively. Therefore, the connection solder bumps 14 have a function of terminals for connecting the semiconductor device to an outside circuit.

When the semiconductor device 10 is mounted on a circuit board, first, the semiconductor device 10 is put on the circuit board 20. The circuit board 20 has

radiation pads 21 located in corresponding position to the radiation solder bumps 13 as shown in Fig. 5. The circuit board 20 further has connection pads 22 located in corresponding position to the connection solder bumps 14 as shown in Fig. 6. Then, the semiconductor device and the circuit board are subjected to the heat treatment (reflow step). The radiation solder bumps 13 and connection solder bumps 14 are melted by the heat treatment so that both of the solder bumps 13, 14 are connected and joined to the radiation pads 21 and the connection pads 22, respectively. Therefore, the semiconductor device 10 is fixed on the circuit board 20.

Since each of the connection solder bumps 14 is connected to one of the electrodes of the semiconductor chip, the connection solder bumps 14 should be connected to the connection pads 22 individually. Therefore, as shown in Figs. 1 and 2, the connection solder bumps 14 are located with a predetermined pitch or distance so that the adjacent connection bumps 14 should not joined each other by the heat treatment (the joining of pumps is called as a solder bridge).

On the other hand, the radiation solder bumps 13 are located with a smaller pitch or distance than that of the connection solder bumps' as shown in Figs. 1 and 2. Therefore, the radiation solder bumps 13 are joined each other to form a solder bridge by the heat treatment. As a result, the radiation bumps form a one body connection layer 30 as shown in Fig. 3. In the first embodiment, the connection layer 30 for an outgoing radiation is connected to the individual radiation pads 21.

For example, diameter of the radiation solder bumps 13 and the connection solder bumps 14 is 0.75mm, the pitch or distance between the radiation solder bumps 13 is 1.00mm and the pitch or distance between the connection solder bumps 13 is 1.27mm. Preferably, the pitch or distance between the radiation solder bumps 13 is 1 to 1.4 times of the diameter of the radiation solder bumps 13. Also, the pitch or distance between the connection solder bumps 14 is

1.6 to 1.7 times of the diameter of the connection solder bumps 14.

In the structure shown in Fig. 3, heat energy generated in the semiconductor chip during the operation is transferred to the circuit board 20 through the connection layer 30. The transferred heat energy is diffused in the circuit board 20 and outgoing from the circuit board 20. At this time, since a thermal conduction part from the semiconductor device 10 to the circuit board 20 is comprised of a joining connection layer 30, an effective area ratio for outgoing radiation is higher than that of the conventional semiconductor device structure. Therefore, radiation efficiency of the semiconductor device according to the first embodiment of the present invention is improved.

For the purpose of joining the adjacent radiation solder bumps 13 easily, a ratio of the effective area of the radiation pads 21 to all area thereof should be higher than a ratio of the effective area of the connection pads 22 to all area thereof. For example, as shown in Figs. 5 and 6, a solder resist layer 40 having openings 41 and 42 are formed on the surface of the circuit board 20. In such case, the opening 41 for the radiation pad 21 should have larger diameter d2 (shown in Fig. 5) than a diameter d1 of the opening 42 for the connection pad 22 as shown in Fig. 6.

The diameter d1 of the opening 42 for the connection pads 22, that is an effective area ratio, is determined so that the adjacent connection solder bumps are not joined each other. On the other hand, the effective area ratio for the radiation pads 21 is set to higher than that for the connection pads 22 so as to form the solder bridge easily. Where the diameter of the opening 41 is relatively bigger, the diameter of the radiation bumps 13 can be bigger and the solder bridge is easily formed.

Figure 7 is a side elevation view of a semiconductor device and a circuit board according to the second embodiment of the present invention. Figure 8 is a bottom plan view of the semiconductor device according to the second

embodiment of the present invention. Figure 9 is an enlarged elevation view of the semiconductor device and the circuit board shown in dotted square in Fig. 7. In the second embodiment, the semiconductor 10 has the same structure of the first embodiment. The circuit board 20 of the second embodiment has a radiation pad 23 having a wide continued area covering the central area of the back surface of the substrate 11a.

In the second embodiment, the connection layer 30 of the semiconductor device 10 is joined with the radiation pads entirely. Therefore, thermal conduction efficiency between the connection layer 30 and the circuit board 20 is larger than that of the first embodiment. So, the heat energy generated in the semiconductor chip is transferred to the circuit board effectively.

Figure 10 is a sectional view of a semiconductor device 50 according to the third embodiment of the present invention. In the third embodiment, a substrate 51a has a radiation board 53 in the central area on the back side thereof. The radiation board has a high coefficient of thermal conductivity for transferring heat energy from a semiconductor chip 52 molded by the package 51 to radiation solder bumps 54 which are formed on the radiation board 53. The connection solder bumps are formed in the peripheral area of the substrate 51a. Bonding wires 56 connect the electrodes of the semiconductor chip 52 and the conductive lines formed in the substrate 51a, respectively. As explained in the first embodiment, each of the conductive lines is connected to the connection solder bumps 55, respectively. The pitches or distances between the radiation solder bumps 54 and between the connection solder bumps 55 are the same to the first embodiment.

In the third embodiment, the heat energy generated in the semiconductor chip 52 is effectively transferred to the radiation solder bumps 54 through the radiation board 53. When the radiation solder bumps 54 are turned to the connection layer by the heat treatment and the connection layer is connected to

the circuit board, higher radiation efficiency than that of the first embodiment is obtained.

Figure 11 is a sectional view of a semiconductor device 50 according to the fourth embodiment of the present invention. The semiconductor device 50 of the fourth embodiment is added a transit portion 53a to the semiconductor device of the third embodiment. The transit portion 53a is directly contacted to a semiconductor chip 52 and a radiation board 53. The transit portion 53a is formed of a material having high coefficient of thermal conductivity. Other portions of the fourth embodiment are same to the third embodiment.

In the fourth embodiment, the energy generated in the semiconductor chip 52 is transferred to the radiation board 53 through the transit portion 53a. Therefore, higher radiation efficiency than that of the third embodiment is obtained.

Figure 12 is a sectional view of a semiconductor device 50 according to the fifth embodiment of the present invention. The semiconductor device 50 of the fifth embodiment has a plane transit portion 53b instead of the transit portion 53a of the fourth embodiment. The plane transit portion 53b is directly contacted to a semiconductor chip 52 and a radiation board 53. The plane transit portion 53b is formed of a material having high coefficient of thermal conductivity. Other portions of the fifth embodiment are same to the fourth embodiment.

In the fourth embodiment, the energy generated in the semiconductor chip 52 is transferred to the radiation board 53 through the plane transit portion 53b. Since the plane transit portion 53b is contacted to the semiconductor chip 52 and the radiation board 53 with larger area than the transit portion 53a, higher radiation efficiency than that of the fourth embodiment is obtained.

Further, the semiconductor chip 52 can be directly contacted to the radiation board 53 without the transit portion 53b. In this case, the semiconductor chip 52 is joined with the radiation board 53 by die bonding material.

Figure 13 is a sectional view of a semiconductor device 60 according to

the sixth embodiment of the present invention. In the sixth embodiment, the semiconductor device 60 has a substrate 62 having a recess on the back surface 62a thereof. The semiconductor chip 61 is mounted in the recess of the substrate 62 by the chip-on board mounting (COB) method so that electrodes of the semiconductor chip are connected to conductive lines (not shown in Fig. 13) formed in the substrate 62. Radiation solder bumps 63 are formed on the back surface of the semiconductor chip 61 directly. Connection solder bumps 64 are formed on the back surface 62a of the substrate 62 in order to be connected to the conductive lines, respectively. The pitches or distances between the radiation solder bumps 63 and between the connection solder bumps 64 are the same to the first embodiment.

In the sixth embodiment, the heat energy generated in the semiconductor chip 61 is directly transferred to the radiation solder bumps 63.

Figure.14 is a sectional view of the semiconductor device according to the seventh embodiment of the present invention. In the seventh embodiment, a peripheral area of the substrate 62 and connection solder bumps have the same structure of the sixth embodiment. Therefore, explanation of these portions are omitted from the drawing (Fig. 14) and the specification.

In the seventh embodiment, a solder resist layer 65 having openings 66 is formed on the back surface of the semiconductor 61 and the back surface 62a of the substrate 62. The opening are located to the corresponding positions for the radiation solder bumps 63 (located on the back surface of the semiconductor ship 61) and for the connection solder bumps (not shown; located in the peripheral area of the back surface 62a of the substrate 62). As shown in Fig. 14, the radiation solder bumps 63 are formed at the designed position which is led from the opening 66. The radiation solder bumps 63 are positioned closely each other for joining in one body during the heat treatment. Where the position of the radiation solder bumps 63 is deviated from the designed position, the solder bumps 63 are joined

before the heat treatment. In such case, a height of the joined radiation solder bumps 63 turns low and such bumps may not be contacted to the circuit board. However, in the seventh embodiment, the radiation solder bumps 63 are formed at the position of the opening 66 of the solder resist layer 65 so that the radiation solder bumps 63 are formed in the designed positions and the radiation solder bumps 63 have the same height. Therefore, the radiation solder bumps 63 of the seventh embodiment can be contacted to the circuit board surely.

As explained above, according to the present invention, the semiconductor device has radiation protrude electrodes joining to one body connection layer by the heat treatment. Therefore, effective area for outgoing radiation is increased and radiation efficiency is improved.

WHAT IS CLAIMED IS:

1. A package structure for a semiconductor device comprising:

a substrate having a main surface and a back surface;

a semiconductor chip formed on the main surface of said substrate;

a package covering said semiconductor chip;

a plurality of radiation protrude electrodes formed on the back surface of said substrate in a chip area where said semiconductor chip is located, each of said radiation protrude electrodes formed with a first pitch so that said radiation protrude electrodes make one body joining layer when the package structure is subjected to a heat treatment; and

a plurality of connection protrude electrodes formed on the back surface of said substrate in a peripheral area of the chip area, each of said connection protrude electrodes formed with a second pitch which is larger than the first pitch so that said connection protrude electrodes stay individual when the package structure is subjected to a heat treatment.

2. A package structure according to claim 1, wherein said radiation protrude electrodes and connection protrude electrodes are solder bumps.

3. A package structure according to claim 1, wherein said connection protrude electrodes are electrically connected to pads of said semiconductor chips.

4. A package structure according to claim 1, wherein said substrate includes radiation plate high coefficient of thermal conductivity formed on the back surface in the chip region of said substrate, and wherein said radiation protrude electrodes are formed on the radiation plate.

5. A package structure according to claim 4, wherein said substrate has a relay portion having high coefficient of thermal conductivity attached said semiconductor chip and the radiation plate.

6. A package structure according to claim 5, wherein said relay portion is attached entire back surface of said semiconductor chip.

7. A package structure according to claim 1, wherein said radiation protrude electrodes and connection protrude electrodes have the same diameter.

8. A package structure according to claim 7, wherein the first pitch is about 1 to 1.4 times of the diameter of the electrodes, and the second pitch is about 1.6 to 1.7 times of the diameter of the electrodes.

9. A method of mounting a semiconductor device on a circuit board comprising the step of:

providing the semiconductor device including,

a plurality of radiation protrude electrodes formed on a back surface of a substrate in a chip area where a semiconductor chip is located, each of said radiation protrude electrodes formed with a first pitch, and

a plurality of connection protrude electrodes formed on the back surface of said substrate in a peripheral area of the chip area, each of said connection protrude electrodes formed with a second pitch which is larger than the first pitch;

providing the circuit board including a radiation pad located in corresponding position to the radiation protrude electrodes and a plurality of connection pads located in corresponding position to the connection protrude electrodes;

mounting the semiconductor device to the circuit board so that the radiation protrude electrodes are contacted to the radiation pad and that the connection protrude electrodes are contacted to the connection pads; and

subjecting the mounted semiconductor device to a heat treatment so that the radiation protrude electrodes make one body joining layer and that the connection protrude electrodes stay individual.

10. A method of mounting a semiconductor device according to claim 9, wherein said radiation protrude electrodes and connection protrude electrodes are solder bumps.

11. A method of mounting a semiconductor device according to claim 9, wherein said radiation protrude electrodes and connection protrude electrodes have the same diameter.

12. A method of mounting a semiconductor device according to claim 11, wherein the first pitch is about 1 to 1.4 times of the diameter of the electrodes, and the second pitch is about 1.6 to 1.7 times of the diameter of the electrodes.

13. A method of mounting a semiconductor device according to claim 9, wherein the radiation pad has a plurality of radiation pads located at the corresponding positions to the radiation protrude electrodes.

14. A method of mounting a semiconductor device according to claim 9, wherein the radiation pad has an area covering the chip area of the substrate.

15. A package structure for a semiconductor device comprising:

a substrate having a main surface and a back surface, said substrate

having a recess on the back surface;

a semiconductor chip formed in the recess of said substrate so that a back surface of said semiconductor chip and the back surface of said substrate constitute the same plane substantially;

a plurality of radiation protrude electrodes formed on the back surface of said semiconductor chip, each of said radiation protrude electrodes formed with a first pitch so that said radiation protrude electrodes make one body joining layer when the package structure is subjected to a heat treatment; and

a plurality of connection protrude electrodes formed on the back surface of said substrate, each of said connection protrude electrodes formed with a second pitch which is larger than the first pitch so that said connection protrude electrodes stay individual when the package structure is subjected to a heat treatment.

16. A package structure according to claim 15, wherein said radiation protrude electrodes and connection protrude electrodes are solder bumps.

17. A package structure according to claim 15, wherein said connection protrude electrodes are electrically connected to pads of said semiconductor chips.

18. A package structure according to claim 15, wherein said radiation protrude electrodes and connection protrude electrodes have the same diameter.

19. A package structure according to claim 18, wherein the first pitch is about 1 to 1.4 times of the diameter of the electrodes, and the second pitch is about 1.6 to 1.7 times of the diameter of the electrodes.

Abstract of the Disclosure

A package structure for a semiconductor device comprises a substrate having a main surface and a back surface, a semiconductor chip formed on the main surface of the substrate, a package covering the semiconductor chip, radiation protrude electrodes and connection protrude electrodes. The radiation protrude electrodes are formed on the back surface of the substrate in a chip area where said semiconductor chip is located. Each of the radiation protrude electrodes are formed with a first pitch so that the radiation protrude electrodes make one body joining layer when the package structure is subjected to a heat treatment. The connection protrude electrodes are formed on the back surface of the substrate in a peripheral area of the chip area. Each of the connection protrude electrodes formed with a second pitch which is larger than the first pitch so that the connection protrude electrodes stay individual when the package structure is subjected to a heat treatment.

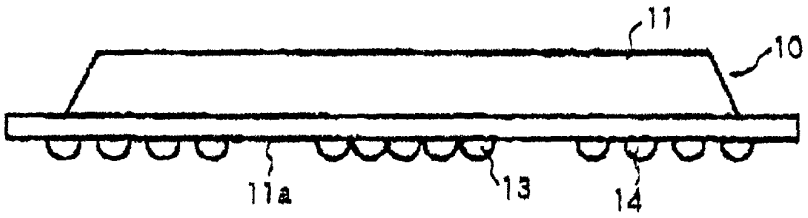

Fig. 1

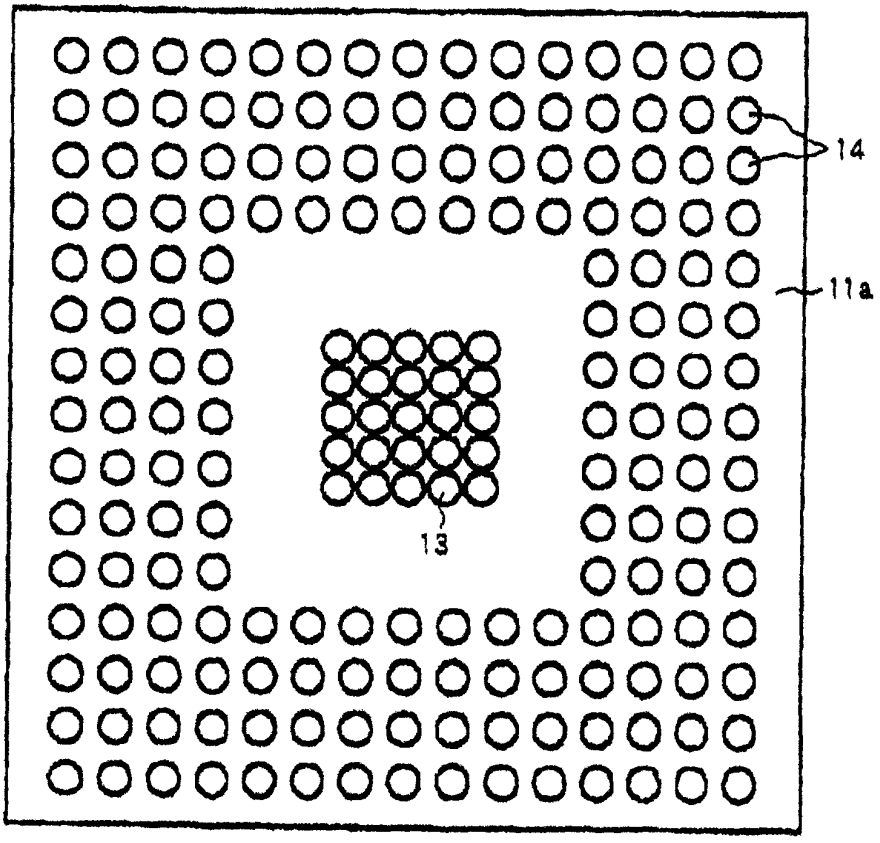

Fig. 2

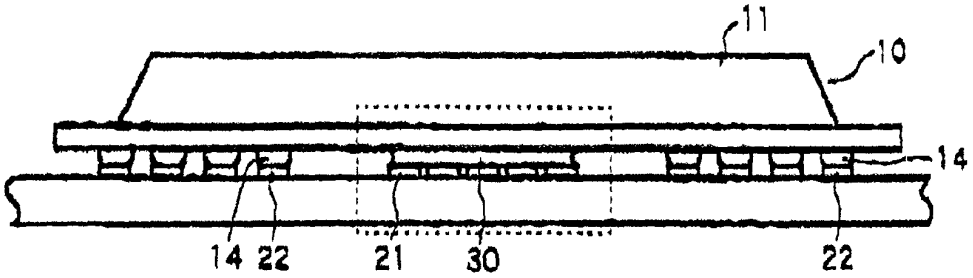

Fig. 3

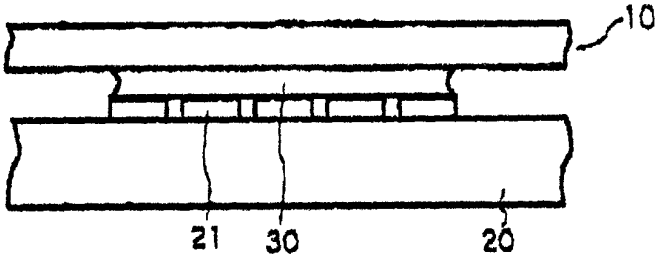

Fig. 4

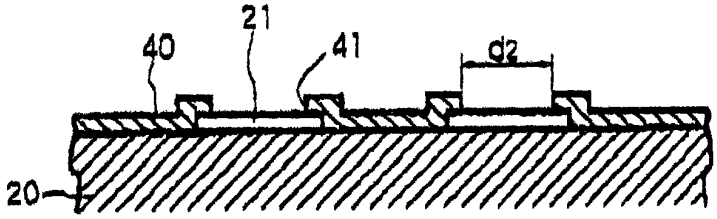

Fig. 5

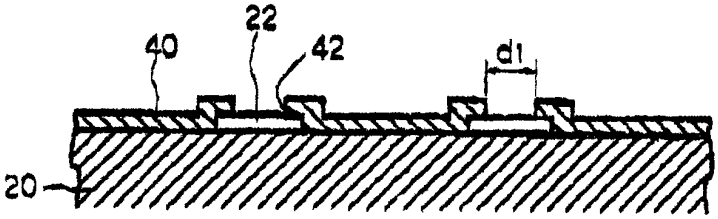

Fig. 6

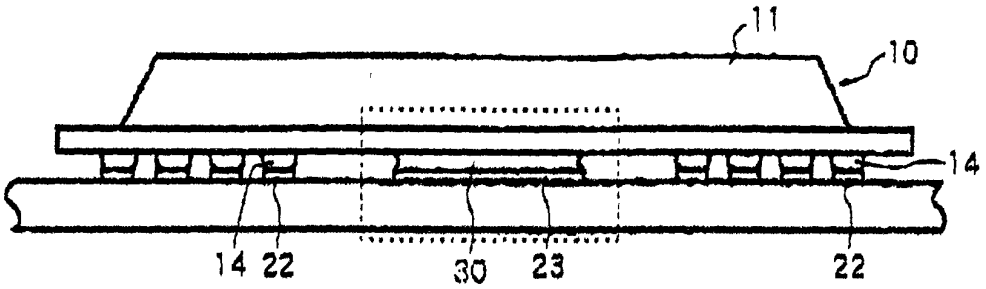

Fig. 7

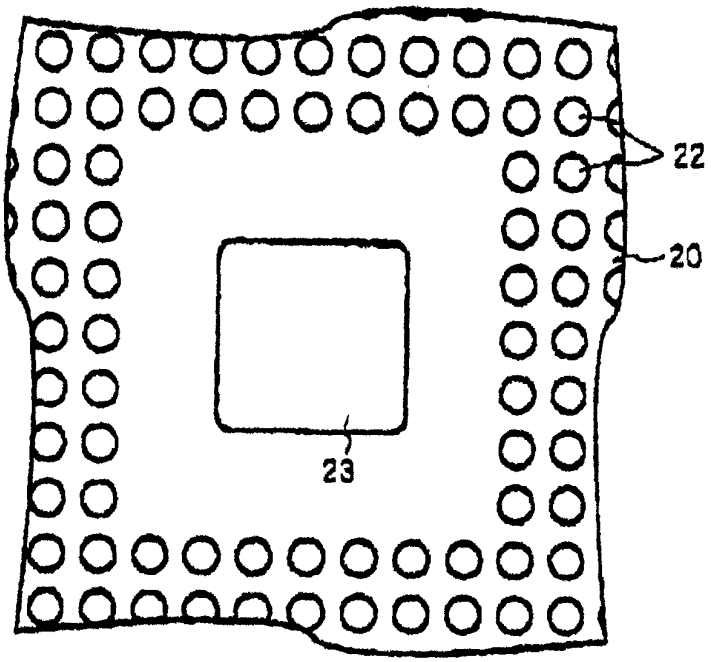

Fig. 8

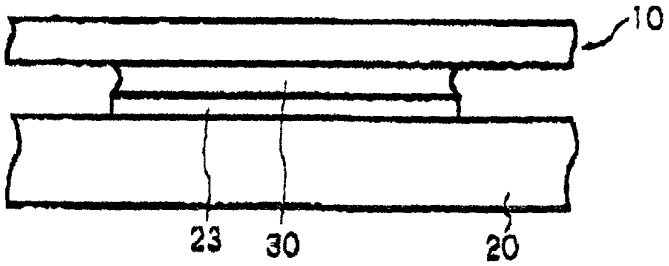

Fig. 9

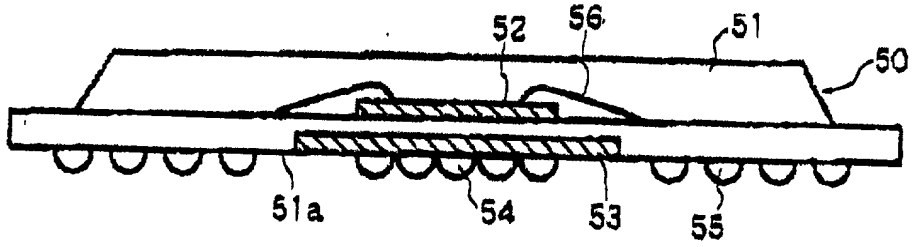

Fig. 10

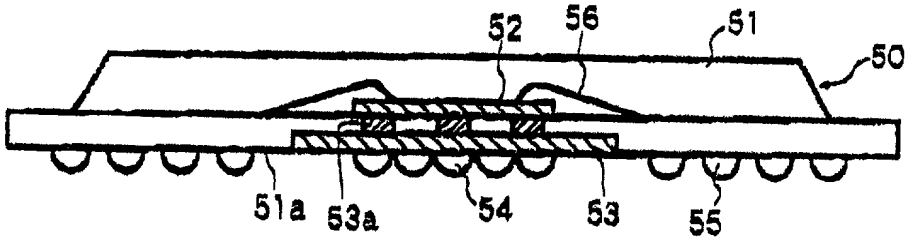

Fig. 11

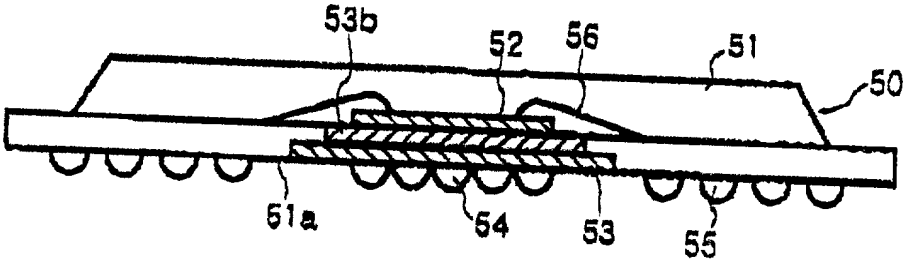

Fig. 12

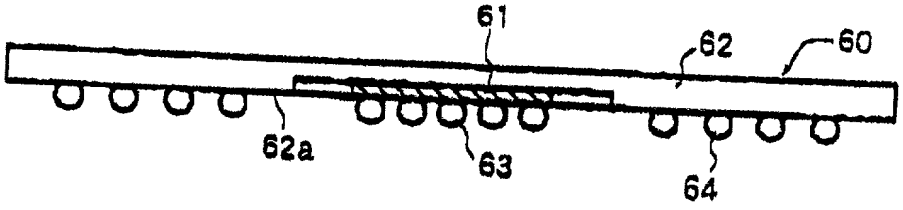

Fig. 13

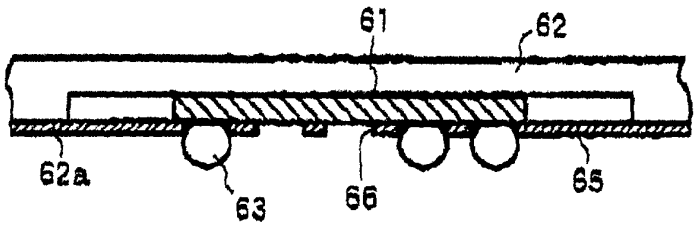

Fig. 14

97-1

Attorney Reference_____

DECLARATION FOR UNITED STATES PATENT APPLICATION, POWER OF ATTORNEY, DESIGNATION OF CORRESPONDENCE ADDRESS

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name, and that I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

PACKAGE STRUCTURE FOR A SEMICONDUCTOR DEVICE

the specification of which
[x] is attached hereto,
[ ] was filed on_____, as Application Serial No. _____,
and was amended on _____ (if applicable);
[ ] was filed under the Patent Cooperation Treaty on_____,
Serial No. _____, the United States of America being designated.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose to the Patent and Trademark Office information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent, utility model, design or inventor's certificate listed below and have also identified below any foreign application(s) for patent, utility model, design or inventor's certificate having a filing date before that of the application(s) on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
Number	Country	Date Filed	Yes	No
232126/98	JAPAN	August 18, 1998	X	

I hereby appoint the following attorneys to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith: Steven M. Rabin (Reg. No. 29,102), Thomas M. Champagne (Reg. No. 36,478), Christopher H. Lynt (Reg. No. 33,619) and Robert H. Berdo, Jr. (Reg. No. 38,075), 1725 K Street, N.W., Washington, D.C. 20006, Telephone: (202) 659-1915; Fax: (202) 659-1698. Address all correspondence to RABIN, CHAMPAGNE & LYNT, P.C., 1725 K Street, N.W., Suite 1111, Washington, D.C. 20006.

The undersigned hereby authorizes the U.S. attorneys named herein to accept and follow instructions from the undersigned's assignee, if any, and/or, if the undersigned is not a resident of the United States, the undersigned's domestic attorney, patent attorney, patent agent, or patent representative as to any action to be taken in the Patent and Trademark Office regarding this application without direct communication between the U.S. attorneys and the undersigned. In the event of a change in the person(s) from whom instructions may be taken, the U.S. attorneys named herein will be so notified by the undersigned.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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